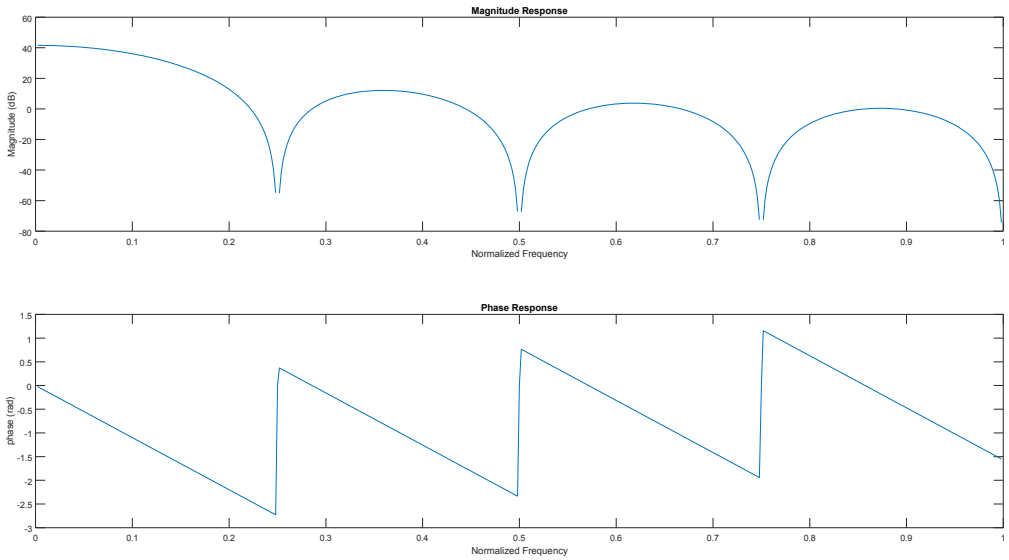
ELE 448 Final Project

Due date: TBD

I. Introduction:

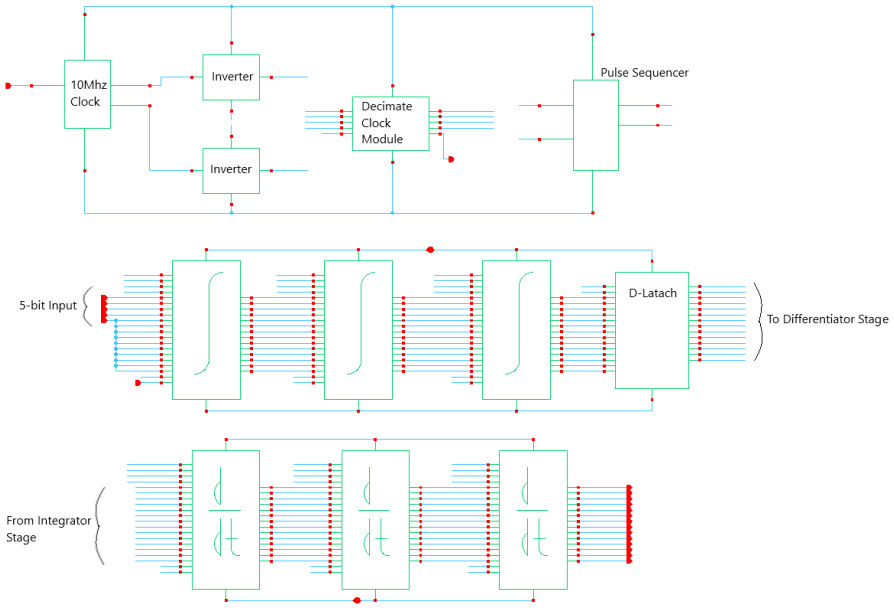
For the final project, a 3 stage, 5-bit cascaded integrator-comb (CIC) filter will be designed. Comb filters can be defined as adding a delayed version of a signal to itself. They get their name from the comb-like appearance of their magnitude response. An example of this can be seen below:



This filter is of 8th order and has the following transfer function:

$$H_8(z) = 1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + z^{-5} + z^{-6} + z^{-7} = \frac{1 - z^{-8}}{1 - z^{-1}}$$

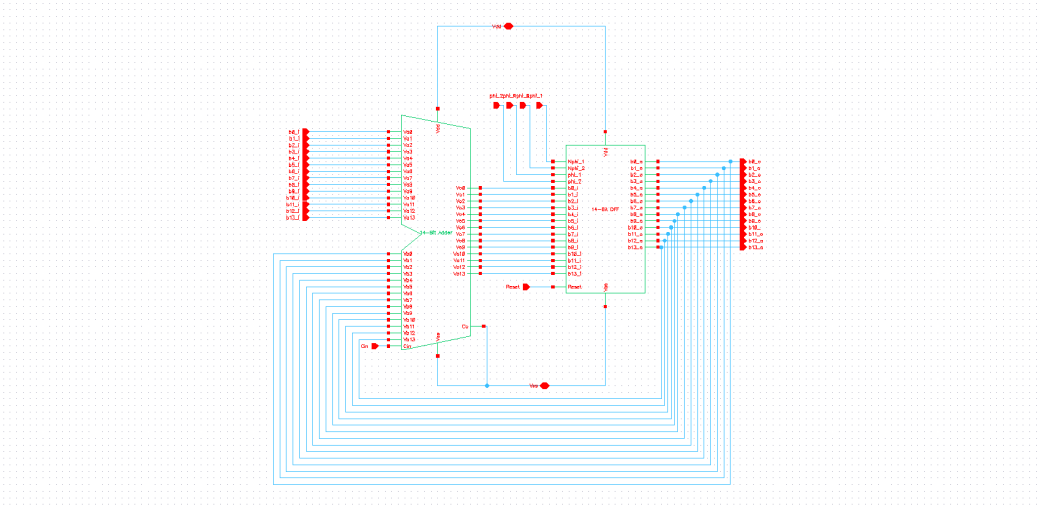
In order to enable enough room for shifting the 5-bit input, a 14-bit input register is required. This means that the lower 5-bits of this input register will contain the data and bit 4 will be sign extended onto bits 5-13 of the register due to the fact that the input is a signed number. It is assumed that the input to this filter is of 2's compliment. This 14-bit register is then the input to an integrator. Since this is a 3-stage filter, 3 integrators will be cascaded together. These integrators operate at the sampling clock which should be 10MHz. The output of the integrator stage will connect to a 14-bit D-Latch that operates every 8 clock cycles of the sample clock. To ensure that this latch only updates its outputs every 8 clock cycles, it needs a clock signal that has a frequency of $1.25\ MHz$ and only lasts for one cycle of the sampling clock. The output of the D-Latch then connects to a 14-bit differentiator. Again, since this is a 3-stage filter, 3 differentiators are cascaded together. These differentiators will run at a decimated clock due to the fact that they only receive an input every 8th clock cycle of the sampling clock. The decimated clock can be realized by use of a 4-bit counter. A schematic for the comb filter can be seen below:



The main parts of this filter consist of an integrator, differentiator, and clocking system. As a result, in order to build it, we need to know how these components work. A digital integrator is known to have the following transfer function:

$$\frac{V_o}{V_i} = H(z) = \frac{1}{1-z^{-1}}$$

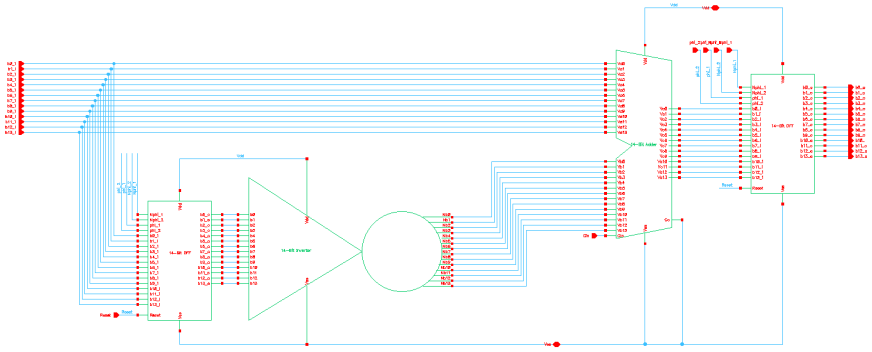
Which tells us that $V_o(1-z^{-1}) = V_i$ or in the discrete-time domain, $V_o(n) = V_i(n) + V_o(n-1)$. In words, the current output that is seen is equal to the sum of the current input and the previous output. As a result, in order to implement an integrator, we need to have an adder and a delay element (D-Flip-Flop). A schematic of a 14-bit integrator can be seen below:



A differentiator, on the other hand, does not have any feedback. This is apparent by its transfer function.

$$\frac{V_o}{V_i} = H(z) = 1 - z^{-1}$$

By a similar analysis to the integrator, it can be seen that $V_o(n) = V_i(n) - V_i(n-1)$. As a result, in order to implement a differentiator, we need to subtract the previous input from the current input. The subtraction can be realized with an adder by utilizing the fact that the input is of 2's compliment. More specifically, if we invert all the bits of the delayed version of the input and add 1 by connecting the carry in on the adder to V_{dd}, then we are in fact performing a subtraction operation. The schematic of a 14-bit differentiator is illustrated below:



It is important to note that the Flip-Flops being used have a reset. All the resets should be tied together and should be utilized in the simulation. Before sending an impulse into your comb filter be sure to reset the Flip-Flops by applying a reset signal for at least 1 cycle of both two-phase clocks.

II. Assignments:

1. Create your own block diagram of the comb filter
    a. Show clocks

2. 14-Bit Full Adder; used for both the integrators and differentiators
    a. Create a schematic
    b. Create a symbol

3. 14-Bit DFF; used for both integrators and differentiators
    a. Create a schematic
    b. Create a symbol

4. 14-bit Inverter; used for the differentiators
    a. Create a schematic
    b. Create a symbol

5. 14-bit D Latch
    a. Create a schematic
    b. Create a symbol

6. Integrator; consists of a 14-bit adder and 14-bit DFF
    a. Create a schematic
        i. One input for the adder will come from a 14-bit input and the other input will be feedback from the DFF output
        ii. The input to the DFF will come from the output of the adder
        iii. The carry out of the adder is not used
        iv. The output of the DFF is the output of the integrator
    b. Create a symbol
    c. Simulate the inverter by applying a logic high to the least significant bit
        i. What do you expect to see at the output?
7. Differentiator; consists of 2 14-bit DFFs, a 14-bit inverter, and a 14-bit adder
    a. Create a schematic
        i. The 14-bit input will be connected to both an input of the adder and a DFF
        ii. The output of the DFF mentioned in (i) will connect to the input of the inverter
        iii. The output of the inverter will connect to the other input of the adder
        iv. The output of the adder will connect to the other DFF
        v. The output of the DFF will be the differentiator output
    b. Create a symbol

8. Clocks
    a. Create a test cell for the clocks
        i. A two-phase clock with inverters operating at the sampling frequency is needed
        ii. A two-phase decimated by 8 clock is needed for the differentiators
            1. The sampling clock can be decimated by using a 4-bit counter
        iii. A pulseSequencerSingle_180 cell is needed to generate the D Latch pulse
            1. The sampling clock should be connected to the V_Clk_in input and the decimated clock should be connected to the other input
    b. Test the comb filter clocks
        i. Does the simulation results make sense?

9. Comb Filter
    a. Create a schematic using the components that were created in the previous steps
    b. Create a symbol
    c. Test the comb filter
        i. The simulation results should be symmetrical due to the filters linear phase

ii. In order to know if your filter is working properly, an impulse can be sent into the system and compared to an impulse response obtained via MatLab
    1. The impulse must be clocked by a single clock edge
iii. The comb filter that is being designed has the following impulse response:

'000001'
'000011'
'000110'
'001010'
'001111'
'010101'
'011100'
'100100'
'101010'
'101110'
'110000'
'110000'
'101110'
'101010'
'100100'
'011100'
'010101'
'001111'
'001010'
'000110'
'000011'
'000001'

iv. Note that there will be some delay before the first value is realized
v. Due to the fact that the comb stage is being decimated by 8, every 8th output will be realized

III. Report:

A report is required for this project. It is expected that you describe each component of your design in detail as well as the overall filter in a similar manor to the reports you have been handing in throughout the semester. It is normal for a design to not produce expected simulation results on the first try. As a result, there should be a section in your report about your process to solve the problems.